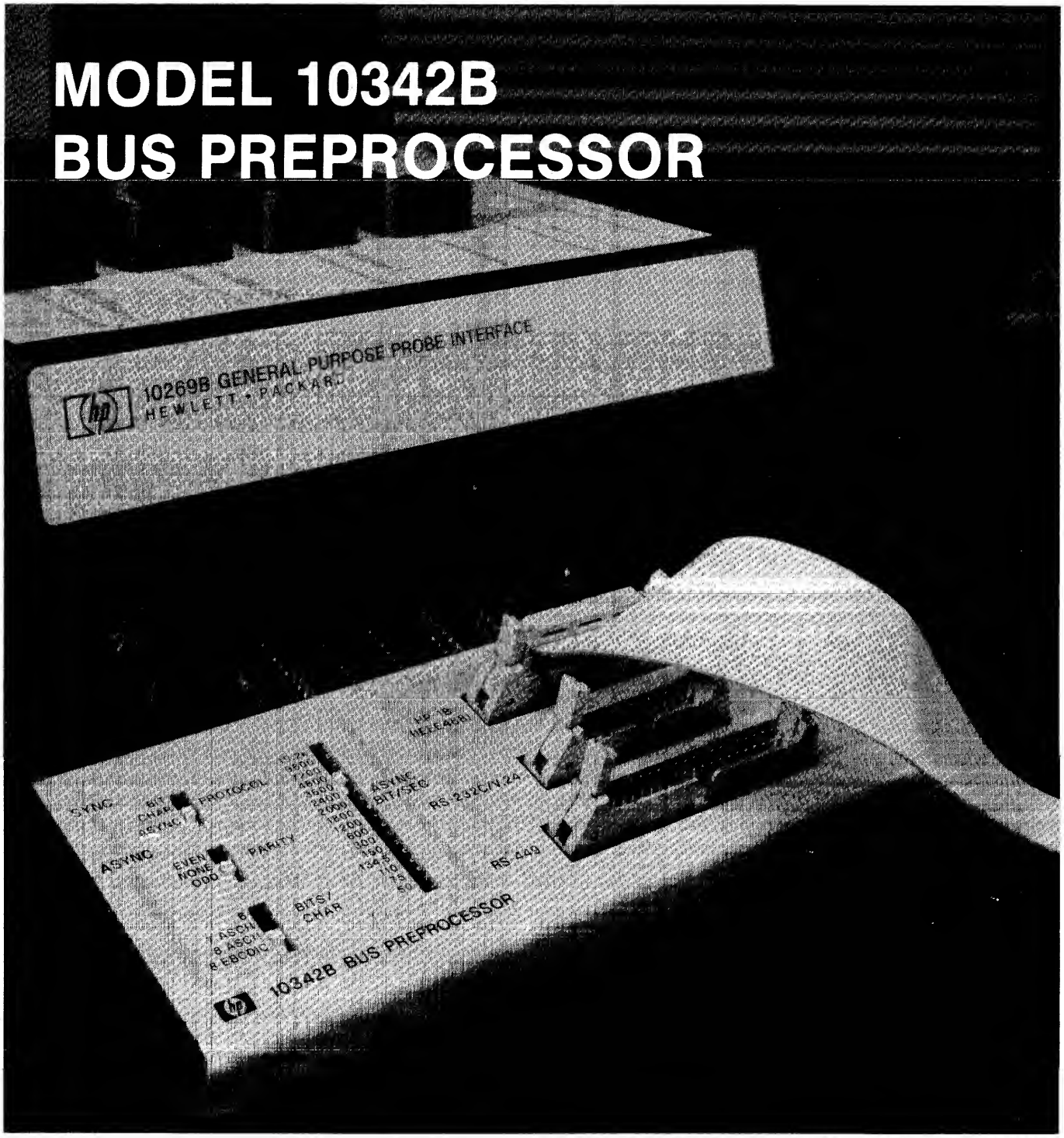
OPERATING MANUAL

MODEL 10342B
BUS PREPROCESSOR



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MODEL 10342B
BUS PREPROCESSOR

Manual Part No. 10342-90901
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CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

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For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CWA584

10342B Operating Manual

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Chapter 1
GENERAL INFORMATION

INTRODUCTION

The HP 10342B Bus Preprocessor, with the HP 10269A or HP 10269B General Purpose Probe Interface, provides an easy connection between the HP 1630A/D/G or HP 1631A/D Logic Analyzers and three popular data buses, HP-IB (Hewlett-Packard's implementation of IEEE 488-1978), RS-232-C/CCITT V.24, or RS-449. Software supplied with the HP 10342B provides inverse assembly of activity on the buses and configurations for the logic analyzers.

MANUAL PURPOSE AND ORGANIZATION

The purpose of this manual is to provide information for using the HP 10342B. The extent to which a bus can be analyzed is generally dependent on the model of logic analyzer used. Any information provided in this manual concerning using the logic analyzers is supplementary to that provided in the analyzer operation and programming manual.

Also, this manual does not contain the complete standards for the three buses covered. The appendices contain abbreviated versions of the standards for the buses. Additional information should be obtained from the appropriate standards organization for each bus.

This manual is organized into several chapters.

CHAPTER 1 covers general information such as product description and accessories.

CHAPTER 2 covers general hardware information, such as inspection, power requirements, maintenance, and troubleshooting.

CHAPTER 3 covers general information about the software supplied.

CHAPTER 4 covers use of the HP 10342B for preprocessing the HP-IB. It includes installation and other information specific to using the HP 10342B on this bus.

CHAPTER 5 covers use of the HP 10342B for preprocessing the RS-232-C/CCITT V.24 bus. It includes installation and other information specific to using the HP 10342B on this bus.

CHAPTER 6 covers use of the HP 10342B for preprocessing the RS-449 bus. It includes installation and other information specific to using the HP 10342B on this bus.

APPENDICES provide some of the basic specifications of the three buses handled by the HP 10342B.

PREPROCESSOR DESCRIPTION

The HP 10342B Bus Preprocessor combines the capability for analysis of three popular buses into one instrument. The HP 10342B itself consists of an interface module which plugs into the HP 10269A/B General Purpose Probe Interface. Three connectors on the front panel of the interface module accept cables which connect with the bus being tested. Switches on the front panel are set up to match the parameters of the signals on the bus.

The inverse assembler and configuration files loaded into the logic analyzer from disc set up the basic analysis parameters. The operator can further set up the analyzer to make and process the measurements in other ways. The exact measurement capabilities depend on the analyzer being used.

- HP-IB

  The HP-IB input to the HP 10342B provides one HP-IB defined load to the bus being monitored. The data and handshake

lines of the bus are buffered and run directly to the probe connectors of the HP 10269A/B.

- RS-232-C/CCITT V.24

  The RS-232-C input to the HP 10342B provides one RS-232-C defined load on the bus being monitored. The lines of the bus under test are buffered and applied to circuitry that takes the serial data stream and converts it back into original data and status. It monitors five handshake lines and their status is stored with each character received. Four switches set up the protocol and data rates. A microprocessor controls the functions in the preprocessor.

- RS-449

  The RS-449 input to the HP 10342B provides one RS-449 defined load on the bus being monitored. The lines of the bus are buffered and ORed with the buffered lines from the RS-232-C connector. From that point all the preprocessing in the HP 10342B is the same. RS-449 inverse assembler and configuration files are provided for the logic analyzer however.

OPERATING CHARACTERISTICS

Table 1-1 gives operating characteristics of the HP 10342B.

Table 1-2. Operating Characteristics

RS-232C (V.24)/449

ASYNCHRONOUS

Data Transfer Rates: (bits/second) 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 or 19 200
Parity: Odd, even, or none
Bits per character: 6-bit transcode
7-bit ASCII
8-bit ASCII
8-bit EBCDIC
Stop bits per character: 1, 1.5, 2

SYNCHRONOUS

Data transfer rate: To 72k bits/second
Format: Bit-oriented protocols (BOP)
Synchronous data link control (SDLC)
High-level data link control (HDLC)
X.25 packet mode
Standard network access protocol (SNAP)
Hewlett-Packard data link control (HPDLC)
Burroughs data link control (BDLC)
Advanced data communication control procedure (ADCCP)
Character-oriented protocols (COP)
Binary synchronous communication (BSC)
Digital data communications message protocol (DDCMP)

Selectable: 6, 7, or 8 bits per character
Transmit clock source: Data terminal equipment (DTE) or data circuit-terminating equipment (DCE). Internally selectable on pc-board.

Table 1-2. Operating Characteristics (cont).

DATA/HANDSHAKE

RS-232C/(V.24)

		LABELS	EIA
Data Lines:	Transmit data	(TX)	(BA)
	Receive data	(RX)	(BB)
Handshake Lines:	Request to send	(RTS)[1]	(CA)
	Clear to send	(CTS)[1]	(CB)
	Data set ready	(DSR)[1]	(CC)
	Data terminal ready	(DTR)[1]	(CD)
	Carrier detect	(CD)[2]	(CF)

RS-449

		LABELS
Data Lines:	Send data	(SD)
	Receive data	(RD)
Handshake Lines:	Request to send	(RS)[1]
	Clear to send	(CS)[1]
	Data mode	(DM)[1]
	Terminal ready	(TR)[1]
	Receive ready	(RR)[2]

HP-IB

Data: Data in/out (1 through 8)

		LABELS
Management:	Interface clear	(IFC)
	Attention	(ATN)
	Service request	(SRQ)
	Remote enable	(REN)
	End or identify	(EOI)
Handshake:	Data valid	(DAV)[3]
	Not ready for data	(NRFD)
	Not data accepted	(NDAC)

NOTES: 1. Synchronous 2. Asynchronous 3. Used as Data Clock

GENERAL

Inputs: Three provided: RS-232C/(V.24), RS-449, and HP-IB.

Outputs: Three mini-probe sockets can be connected internally to any of the input lines via jumper wires.

Signal line loading: RS-232C/V.24 and RS-449, 1 standard load; HP-IB, 1 LS load; load is at the end of the supplied ribbon cables.

Power requirement: +5 V at 0.65A

ENVIRONMENTAL

Temperature: Operating, 0° to 55° C (+32° to +131° F);
Non-operating, -40° to +75° C (-40° to +167° F).

Altitude: Operating, up to 4600 m (15 000 ft).
Non-operating, up to 15 300 m (50 000 ft).

Humidity: 90% non-condensing. Avoid sudden, extreme temperature change that could cause condensation within the instrument.

EQUIPMENT SUPPLIED

Equipment supplied with the HP 10342B consists of the following:

Preprocessor Module
One .75 meter (2.5 ft) HP-IB ribbon cable
One .75 meter (2.5 ft) RS-232C/V.24 ribbon cable
One .75 meter (2.5 ft) RS-449 ribbon cable
One 16-pin jumper cable
20 jumper wires
HP 10269B Overlay
Operating Manual

MINIMUM EQUIPMENT REQUIRED

The following is a list of the minimum equipment required in a system using the HP 10342B Bus preprocessor.

HP 1630A/D/G or HP 1631A/D
HP 10269A or HP 10269B
HP 9121D/S or HP 9122D/S
HP 10342B
HP-IB cables for peripherals

Chapter 2
HARDWARE INFORMATION

INTRODUCTION

This chapter contains information about the hardware supplied with the HP 10342B Bus Preprocessor. Inspection, power requirements, maintenance, and set-up of the logic analyzer system are some subjects covered.

INITIAL INSPECTION

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been inspected mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not operate, notify your nearest Hewlett-Packard Sales and Service Office. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for inspection by the carrier.

POWER REQUIREMENTS

The HP 10342B draws power, +5V, from the rear-panel power BNC of the HP 1630/31 Logic Analyzer. It draws approximately .65 amps. A cable is provided in the accessories for the HP 10269A/B.

OPERATOR MAINTENANCE

The only instrument maintenance an operator needs to perform is to keep the instrument clean. Caution must be used in the selection of cleaning agents. Use a mild soap and water solution. Harsh soaps and solvents could damage the painted finish.

CAUTION

Use care when cleaning the panel of the instrument. Soap and solvents could damage parts or contaminate circuitry below. It is better to apply cleaning solutions to a cloth, then wipe the panel, than to wet the surface directly.

CAUTION

Do not use chemical cleaning agents or abrasive cleaners that could damage plastic parts. Recommended cleaning agents are isopropyl alcohol or a 1% solution of mild detergent in water.

TESTING AND TROUBLESHOOTING

There are no established field testing procedures for the HP 10342B. The HP 10342B is on the Blue Stripe board exchange program. If your instrument is inoperative contact the nearest Hewlett-Packard Sales and Service office for assistance.

The circuitry is fairly simple. Standard off-the-shelf parts are used. If you must effect a repair, standard troubleshooting techniques should be sufficient to isolate and correct a problem.

PROBE INTERFACE OVERLAY

On page 2-5 is a reproduction of the HP 10269B overlay. It is full size so it can be reproduced to make a replacement.

REPLACEABLE PARTS

Since the HP 10342B is on the Blue Stripe board exchange program the only replaceable parts are the major parts and cabling.

Table 2-1. Replaceable Parts.

QTY	DESCRIPTION	PART NUMBER
1	Software Disc	10342-13012
1	HP-IB Cable	10342-61603
1	RS-232-C Cable	10342-61601
1	RS-449 Cable	10342-61602
1	Probe Interface Overlay	10342-94301
1	16-pin Jumper Cable	10342-61604
20	Jumper wires	8120-4665
1	PC Board	10342-66501
1	Top cover	10342-04104
1	Bottom plate	10342-04102
12	4-40 Flathead screw	2200-0512
2	Captive screw	1390-0393
2	Retaining ring	0510-0952

SCHEMATICS

The following information is supplied to help the user understand how the HP 10342B impacts timing measurements of serial bus signals and is not intended to be used to troubleshoot an inoperative instrument.

Serial Input Circuits

The input circuitry for one signal from each of the RS-232 and RS-449 buses is shown in figure 2-1. The inputs for the other signals are identical. Both inputs are buffered and supplied to open-collector drivers. The output of an RS-232 driver is wire-ored with the output of the corresponding RS-449 driver and the line is pulled up to +5V.

The RS-232 line receiver has a threshold connection which is connected to ground through 470pF. This supplies noise immunity for RS-232 signals.

Inversion in the RS-232 circuit is done by using an inverting line receiver. In the RS-449 circuit, "inversion" is done by reversing the connections of the two lines for each signal.

Serial Timing Connections

An overall view of the timing connections is shown in figure 2-2. The RS-232 and RS-449 input circuitry (previously covered) is represented by their respective blocks.

The three synchronous clocks from the buses are multiplexed with the two asynchronous clocks generated in the HP 10342B to provide one transmit and one receive clock. Clock selection depends on the internal and front-panel switch settings. The two selected clocks are used by the SIO and also sent to J6 where they join the buffered and inverted serial signals for connection to the logic analyzer timing inputs.

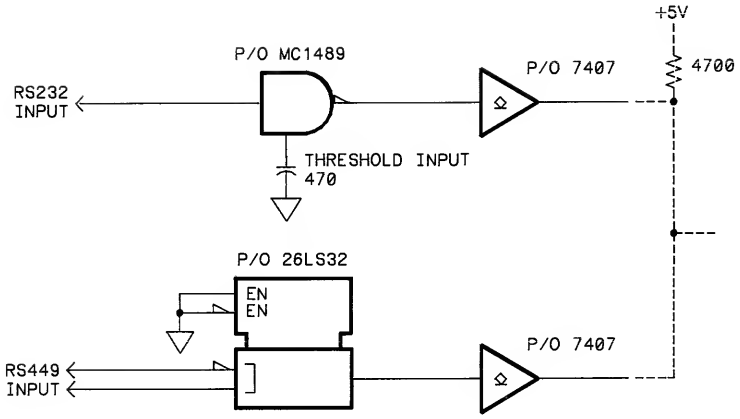


Figure 2-1. Serial Input Circuitry.

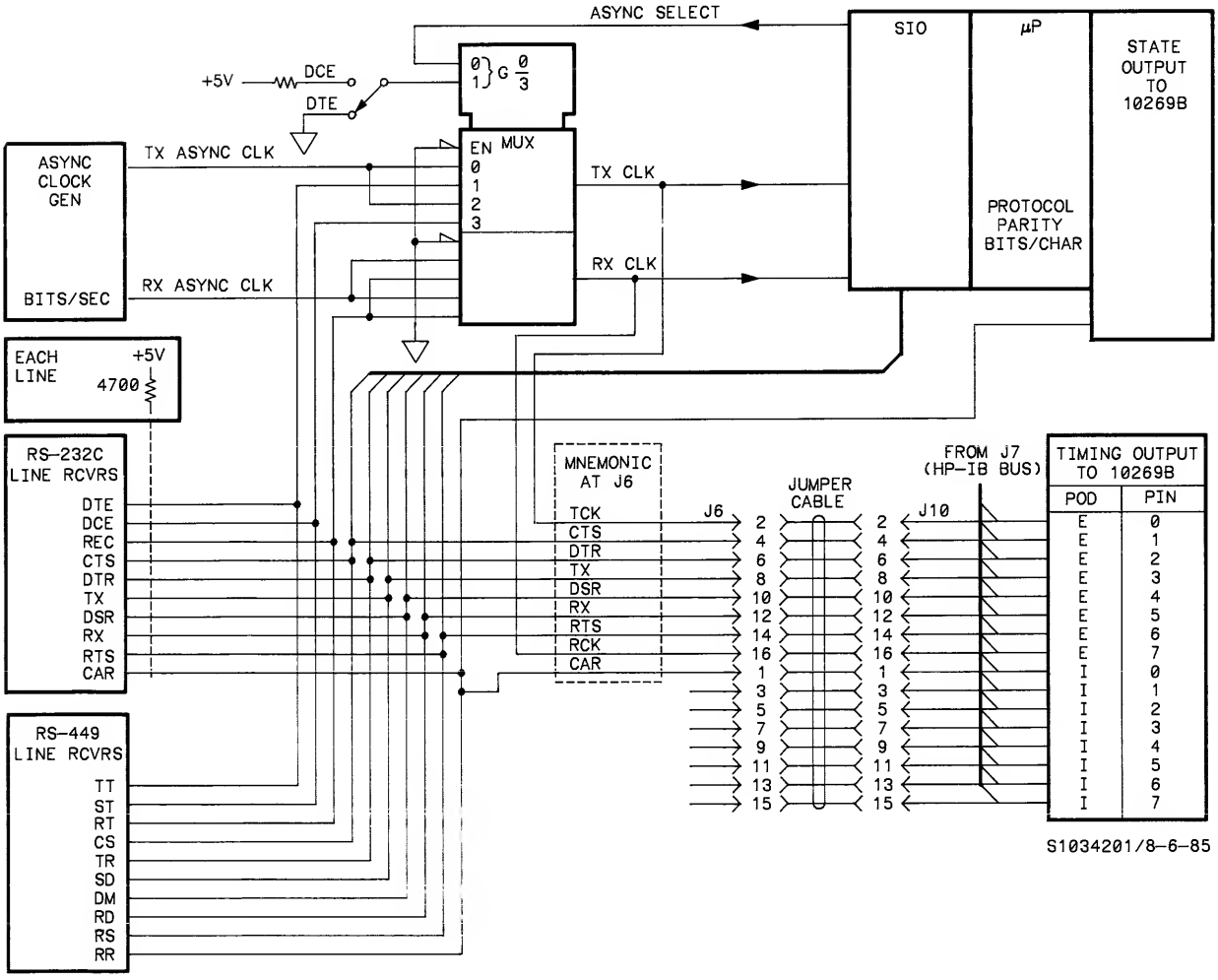


Figure 2-2. Serial Timing Circuitry.

AUXILIARY IN

+5V INPUT

10342

SERIAL	A/D	2	3			1
SERIAL	G	2	3			1
HPIB	A/D			3	4	1
HPIB	G			3	4	1

A B C D E

SERIAL	D	0
HPIB	D	0

F G H I

HEX	CHAR.	HEX	CHAR.	HEX	CHAR.	HEX	CHAR.
00	NUL	0C	FF	18	CAN	24	$
01	SOH	0D	CR	19	EM	25	%
02	STX	0E	SO	1A	SUB	26	&
03	ETX	0F	SI	1B	ESC	27	'
04	EOT	10	DLE	1C	FS	28	
05	ENQ	11	DC1	1D	GS	29	
06	ACK	12	DC2	1E	RS	2A	*
07	BEL	13	DC3	1F	US	2B	+
08	BS	14	DC4	20	space	2C	,
09	HT	15	NAK	21	!	2D	-
0A	LF	16	SYN	22	"	2E	.
0B	VT	17	ETB	23	#	2F	/

HEX	CHAR.	HEX	CHAR.
30	0	58	X
31	1	59	Y
32	2	5A	Z
33	3	5B	[
34	4	5C	\
35	5	5D	]
36	6	5E	^
37	7	5F	_
38	8	60	`
39	9	61	a
3A	:	62	b
3B	;	63	c
3C	<	64	d
3D	=	65	e
3E	>	66	f
3F	?	67	g
40	@	68	h
41	A	69	i
42	B	6A	j
43	C	6B	k
44	D	6C	l
45	E	6D	m
46	F	6E	n
47	G	6F	o
48	H	70	p
49	I	71	q
4A	J	72	r
4B	K	73	s
4C	L	74	t
4D	M	75	u
4E	N	76	v
4F	O	77	w
50	P	78	x
51	Q	79	y
52	R	7A	z
53	S	7B	{
54	T	7C	|
55	U	7D	}
56	V	7E	~
57	W	7F	▒

10342-94301

Chapter 3
SOFTWARE INFORMATION

INTRODUCTION

This chapter contains information about the software supplied with the HP 10342B Bus Preprocessor. There are three types of files on the flexible disc supplied with the HP 10342B. There is a disc copy program for use in duplicating the disc for archive purposes. There are inverse assembly files for set-up of the logic analyzer and disassembly of the bus activity. There are also configuration files for setting up timing functions of the logic analyzer.

Table 3-1 is a composite list of the files in the software provided with the HP 10342B.

Table 3-1. Software File List.

Filename	Type*	Date	Time	File Description*
COPYFILE	prog	XX/XX/XX	XX:XX	Disk File Copy Utility
IHPIB	config			HPIB CONFIG FOR 163XAD
IHPIB	invasm			HPIB INVERSE ASSEM 2519
IHPIBG	config			HPIB CONFIG FOR 1630G
IRS232C	config	SEE NOTE**		RS232C CONFIG FOR 163XAD
IRS232C	invasm			RS232C INVERSE ASSEM. 2519
IRS232G	config			RS232C CONFIG FOR 1630G
IRS449	config			RS 449 CONFIG FOR 163XAD
IRS449	invasm			RS 449 INVERSE ASSEM. 2519
IRS449G	config	XX/XX/XX	XX:XX	RS 449 CONFIG FOR 1630G

NOTES:

* Configuration files for the instrument not being loaded will show up in the "Type" column as being unknown. For example when loading an HP 1630A/D or HP 1631A/D the HP 1630G files will be unknown and there will be no file description. They cannot be loaded.

** Date and Time information may vary depending on the version of the software on the disc.

COPYING FILES

As soon as possible after receiving your instrument you should copy your disc so that you have a back-up copy. Use the copy and keep the original as a back-up.

Copying files is done with the COPYFILE utility program which provides the user with a method of copying HP 1630/31 executable programs, configuration files, and inverse assemblers from one disc to another.

COPYFILE is an extension of the Storage Operations capabilities of the HP 1630/31 which are limited to copying only non executable programs. An example of a non-executable would be a timing file.

To use COPYFILE, load it using the same loading procedure described in the logic analyzer operating manual.

Once the program starts, the logic analyzer display will ask for: copy FROM file name, file TYPE, bus address and unit number. When these have been specified, press INSERT to load the file to be copied. When the copy FROM file has been loaded, the logic analyzer will display all the same information in the copy TO fields as a default. The filename, bus address, and unit number can be respecified if desired, however, the filetype must remain the same as the file being copied. Press INSERT to write the file.

To exit the COPYFILE program, move the cursor to the EXIT field and press either the NEXT [ ] or PREV [ ] key.

Chapter 4
HP-IB BUS PREPROCESSING

INTRODUCTION

The HP-IB is the Hewlett-Packard implementation of IEEE Standard 488-1978. The HP-IB is a parallel bus with eight data lines, three handshake lines and five control lines. A brief overview of HP-IB is given in appendix A.

PREPROCESSOR FUNCTION

The function of the HP 10342B when monitoring the HP-IB is to connect onto the bus, buffer the lines, provide easy connection to the logic analyzer, and provide set-up of logic analyzer menus and inverse assembly of captured data. The HP 10342B can monitor the state of all the signal lines of the HP-IB. Depending on the logic analyzer used, either all 16 lines (using an HP 1630D or HP 1631D) or eight lines (using the HP 1630A, HP 1630G, or HP 1631A) can be monitored for timing information.

The HP 10342B provides a mass-connect feature for connecting the HP-IB lines up to timing channels or individual connections can be made with jumper wires provided. Timing channels are connected directly to the HP-IB without buffering.

Additionally, any HP-IB line can be connected, unbuffered, to one of the three HP 10342B front panel outputs provided. These can be used for connection to an oscilloscope or one of the analog channels or trigger of an HP 1631A/D.

SYSTEM SET-UP

The minimum equipment necessary to use the HP 10342B Bus Preprocessor is as follows:

Logic Analyzer: HP 1630A/D/G* or HP 1631A/D*
  * with HP 1630/31A or HP 1630G only 8 timing channels are available
Probe Interface: HP 10269A* or HP 10269B
  * with the HP 10269A only 8 timing channels are available
Disc Drive: HP 9121D/S or HP 9122D/S
HP-IB cables for peripherals
HP 10342B Bus Preprocessor

Use the following step-by-step procedure to set up the HP-IB Bus Preprocessing system.

Logic Analyzer

SET UP SYSTEM — Set up your logic analyzer system using procedures in your equipment operators manuals. Set-up will depend on the equipment and peripherals you are using.

Bus Preprocessor

The HP 10342B comes from the factory set up for processing HP-IB, therefore some of the following instructions may be redundant if the HP 10342B is being used for the first time.

CONNECT TIMING JUMPER

On the HP 10342B, connect the ribbon jumper cable from J7 to J9. All 16 possible timing channels are connected when the jumper cable is used. See figure 4-1.

If you use the single jumper wires to connect the timing signals be sure to connect them to corresponding pins of J7 and J9 or the data captured will not match the HP 163X setup provided on disc. You would then need to change the HP 163X [Timing] Format Specification menu to match your hook-up.

One reason to make changes in the timing connections is to put different bus lines onto timing inputs 0-3 for edge and glitch triggering. The preprocessor is set up to have ATN, SRQ, IFC, and NDAC on these lines. For further information, see TIMING RECONFIGURATION on page 4-6.

CONNECT FRONT PANEL OUTPUTS

If you want any data or control lines connected to the front panel outputs, use the small jumper wires to connect pins of J10 to pins of J5. See figure 4-1. When using the mass-connect jumper cable the signals at J10 correspond to the mnemonics at J9.

Example: To connect ATN to front panel Output 1, connect a jumper between J10 pod 1 pin 0 (top right) and J5 pin 1.

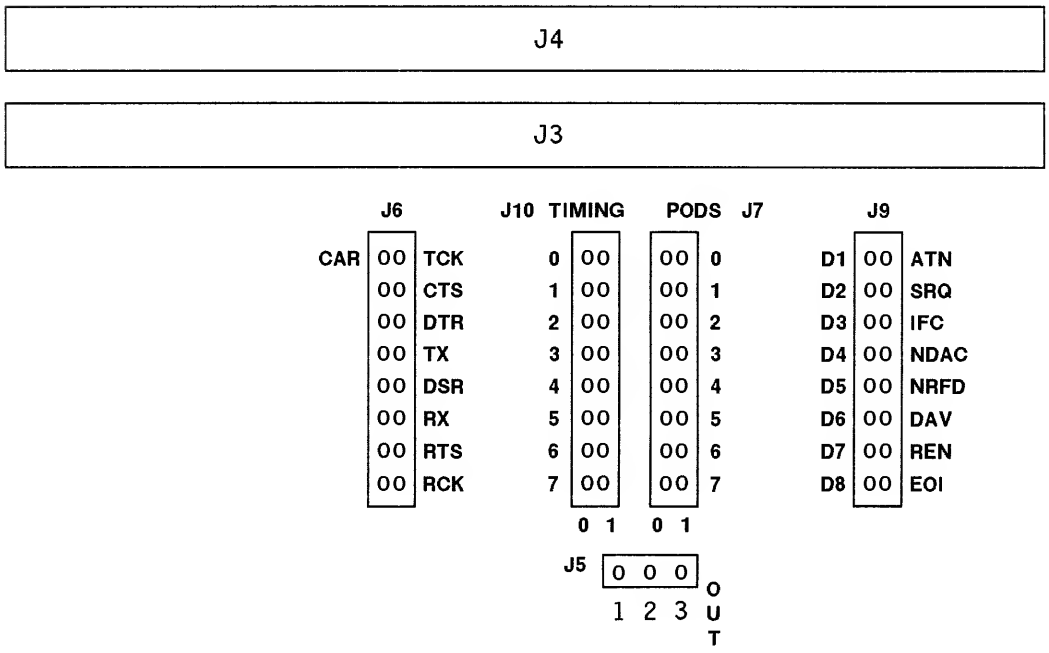


Figure 4-1. HP-IB Timing Connector Locations.

INSTALL PREPROCESSOR

Once all the connections are made, place the HP 10342B at the bottom of the HP 10269 and connect the two 60-pin cables to the connectors on the HP 10342B. Fit the HP 10342B into the bottom of the HP 10269 and fasten them together with the two captive screws.

FRONT PANEL SWITCHES

The front panel switches are used for serial data preprocessing and have no function in preprocessing the HP-IB.

Probe Interface

Though either an HP 10269B or HP 10269A can be used with the HP 10342B, The HP 10269A does not support the additional 8 timing channels of the HP 1630D.

POD CONNECTOR OVERLAY

Lay the HP 10269B overlay over the pod connectors. If you are using an HP 10269A the overlay will be too large to fit well. The overlay shows where pods connect for various logic analyzers and bus preprocessing and gives other useful information.

CONNECT PODS

Connect the logic analyzer pods to the connectors on the HP 10269. If you are using an HP 10269B follow the overlay. For an HP 163XD, POD 3 goes in pod connector C, POD 4 into D, POD 1 into E, and POD 0 into I. For an HP 163XA/G there is no POD 0. If you are using an HP 10269A the connections are the same except there is no pod connector I.

If you are going to be using the HP 10342B on both HP-IB and RS-232-C or RS-449 buses, you can connect logic analyzer POD 2 to pod connector A. You can then switch to serial processing by moving POD 3 to connector B and loading the serial inverse assembler and configuration files.

CONNECT POWER

Connect the BNC to BNC cable supplied with the HP 10269 between the +5V INPUT (ACCESSORY POWER) of the HP 10269 and the +5V (ACCESSORY POWER) output of the logic analyzer.

CONNECT HP-IB CABLE

Connect the HP-IB ribbon cable between the HP-IB bus to be monitored and the HP-IB connector on the HP 10342B.

System Operation

Be sure all the addresses are set on the peripherals before you apply power since most address switch settings are read on power-up.

APPLY POWER

Turn on power for all equipment involved. The logic analyzer comes up in the [Configuration] menu of the System Specification. Press the PREV[ ] key to get the [Storage Operations] menu.

CHECK FOR DISC

Press INSERT to check for the disc drive and display the disc file directory.

LOAD INVASM ROLL the list up to point to the desired file to load. The inverse assembler must be loaded first, so load "IHPIB invasm" by pointing to it, selecting [Load] for an Operation, and pressing INSERT.

LOAD CONFIG Next, load the configuration file "IHPIB config" or "IHPIBG config" depending on your logic analyzer. The instrument will not load the wrong one.

RUN Press RUN. As soon as a clock is available on the bus the logic analyzer will begin to accumulate data.

You may modify the logic analyzer menus to suit the measurement you need to make. Consult your logic analyzer operating manual for further information.

SIGNAL CONNECTIONS

The HP 10342B monitors all HP-IB lines for state information. Eight or 16 lines (depending on the logic analyzer or HP 10269) can be monitored for timing information. Following is a list of the HP-IB signals and where they are input to the analyzer.

Table 4-1. Logic Analyzer to HP-IB Signal Connections.

	STATE			TIMING		
HP-IB LINE	**HP 10269B[1] CONN**	**PIN**	**HP 163X POD**	**HP 10269B[1] CONN**	**PIN**	**HP 163X POD**
DAV	D	J CLK	4			
DIO1	D	0		I	0	0
DIO2	D	1		I	1	
DIO3	D	2		I	2	
DIO4	D	3		I	3	HP 163X ONLY
DIO5	D	4		I	4	
DIO6	D	5		I	5	
DIO7	D	6		I	6	
DIO8	D	7	4	I	7	0
PAR POLL[2]	C	K CLK	3			
ATN	C	0		E	0	1
EOI	C	1		E	7	
REN	C	2		E	6	
IFC	C	3		E	2	
SRQ	C	4		E	1	
NDAC	C	5		E	3	
DAV	C	6		E	5	
NRFD	C	7	3	E	4	1

1. HP 10269A connections are the same except there is no pod connector I (POD 0).
2. Parallel Poll is available but not activated. See CLOCKS in following text.

Clocks

Two clocks are provided to the logic analyzer. These clocks can be ORed to clock data.

DAV DAV, Data Valid, is brought out at HP 10269 pod connector D. Logic analyzer POD 4 is connected there, which provides DAV as the J Clock. The logic analyzer clocks data on the negative edge of the J Clock.

PARALLEL POLL The Parallel Poll clock is brought out at HP 10269 pod connector C. This is the K Clock at logic analyzer POD 3. The PAR POLL clock is ANDed from the EOI and ATN lines of the HP-IB.

The IEEE Standard 488 defines the Parallel Poll to require the EOI and ATN lines to be true for 2μs to be valid. This timing function is not implemented in the HP 10342B.

The configuration file on the disc does not automatically set up the logic analyzer to clock data on parallel polls. To clock data using the ANDed function of EOI and ATN go to the [State] Format Specification menu of the logic analyzer and use the CURSOR and NEXT[ ] keys to put a ↓ symbol under the K in the ORed Clock field. Remember that only data clocked after the 2μs specification is a valid parallel poll.

Status (STAT) Lines

The State Listing monitors the HP-IB interface management (ATN, EOI, REN, IFC, and SRQ) and handshake (NDAC, DAV, and NRFD) lines under the Status label. Only the interface management lines are used in the inverse assembler. All of the lines are displayed in the [State] Waveform Diagram. Table 4-2 shows which HP-IB line corresponds to which Status line.

Table 4-2. Status Lines.

STATUS LINE	HP-IB LINE	STATUS LINE	HP-IB LINE
STAT 0	ATN	STAT 4	SRQ
STAT 1	EOI	STAT 5	NDAC
STAT 2	REN	STAT 6	DAV
STAT 3	IFC	STAT 7	NRFD

Control (CNTRL) Lines

The CNTRL lines are the HP-IB ATN and EOI lines and are the same as the first two STAT lines. They are displayed in the [State] Listing in their user base format.

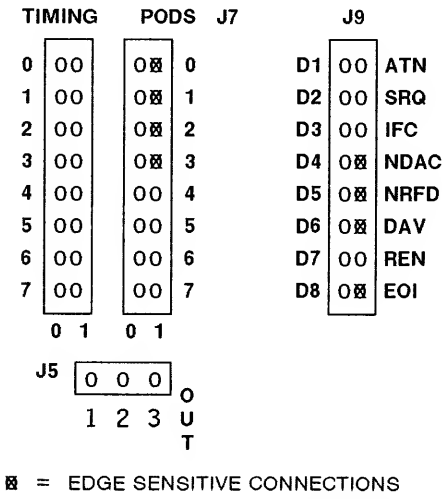
ADDRESS (ADDR)

There is an Address (ADDR) label set up in the [State] Format Specification with one bit from an unused pod assigned to the label . This label is necessary for operation of the logic analyzer but not for use with the HP 10342B. If the ADDR label appears on screen you can go to the [State] List menu and move it off the screen using the SHIFT and ROLL keys. This is done by the configuration file when the software is loaded.

TIMING RECONFIGURATION EXAMPLE

The HP 10342B is factory configured to put ATN, SRQ, IFC, and NDAC on the edge-sensitive channels (0-3) of the timing pod. This is done with the ribbon jumper cable of the HP 10342B and the [Timing] Format Specification menu of the logic analyzer, as set up by the software supplied. Connection of different lines to the edge sensitive timing inputs requires connecting the timing channels with the single jumper wires provided and reconfiguring the menu.

The following example shows how to put NDAC, NRFD, DAV, and EOI onto the edge/glitch timing lines of a logic analyzer with eight timing channels, an HP 1630A, HP 1630G, or HP 1631A. If an HP 1630D or HP 1631D is being used, 16 timing channels with 8 edge-sensitive inputs are available. The method of set-up is the same. The drawing, part of figure 4-1, shows the HP-IB area for jumper connections on the HP 10342B. The accompanying table gives the individual jumper connections to be made.



CONNECT JUMPER	
FROM J7 POD1 PIN	TO J9
0	NDAC
1	NRFD
2	DAV
3	EOI
4	ATN
5	SRQ
6	IFC
7	REN

Figure 4-2. Timing Jumper Reconfiguration.

Change the logic analyzer [Timing] Format Specification channel assignments to those shown below.

```
[Timing] Format Specification----------------------------------------

[Assignment]   Pod1
             [ TTL  ]
             7......0
Activity>    --------
Label  Pol
ATN    [+]  [...*....]
SRQ    [+]  [..*.....]
IFC    [+]  [.*......]
NDAC   [+]  [.......*]
NRFD   [+]  [......*.]
DAV    [+]  [.....*..]
REN    [+]  [*.......]
EOI    [+]  [....*...]
```

Figure 4-3. [Timing] Format Specification Menu Reconfiguration.

Chapter 5
RS-232-C/V.24 BUS PREPROCESSING

INTRODUCTION

The RS-232-C/V.24 is a serial interface with unbalanced data and control lines. A brief overview of RS-232-C/V.24 is given in Appendix C. A comparison between several of the serial interfaces is provided in Appendix B. Further references to RS-232-C should be assumed to include CCITT V.24.

PREPROCESSOR FUNCTION

The primary function of the HP 10342B is to convert the serial data stream into parallel data and status. It monitors five handshake lines and stores their states for each character. Four of the handshake lines are synchronous with the serial controller and one line (carrier detect) is asynchronous but sampled each time a character is output to the logic analyzer.

All lines are buffered at the input to the HP 10342B. The buffers provide one RS-232-C standard load to the bus. Signals are inverted by the buffer circuitry.

The HP 10342B provides a mass-connect feature for connecting the bus lines to timing channels, or individual connections can be made with jumper wires provided. Timing connections are made to the buffered and inverted signals.

Additionally, any buffered line can be connected to one of the three HP 10342B front panel outputs provided. These can be used for connection to an oscilloscope or one of the analog channels or trigger of an HP 1631A/D.

SYSTEM SET-UP

The minimum equipment necessary to use the HP 10342B Bus Preprocessor is as follows:

Logic Analyzer: HP 1630A/D/G* or HP 1631A/D*
* with HP 1630/31A or HP 1630G only 8 timing channels are available
Probe Interface: HP 10269A* or HP 10269B
* with the HP 10269A only 8 timing channels are available
Disc Drive: HP 9121D/S or HP 9122D/S
HP-IB cables for peripherals
HP 10342B Bus Preprocessor

Use the following step-by-step procedure to set up the system for RS-232-C preprocessing.

Logic Analyzer

SET UP SYSTEM

Set up your logic analyzer system using procedures in your equipment operators manuals. Set-up will depend on the equipment and peripherals you are using.

Bus Preprocessor

The HP 10342B comes from the factory set up for processing HP-IB.

CONNECT TIMING JUMPER

On the HP 10342B, connect the ribbon jumper cable to the appropriate pins. All 16 possible timing channels are connected when the jumper cable is connected from J6 to J10. Only nine channels are used with RS-232-C processing. See figure 5-1.

If you use the single jumper wires to connect the timing signals be sure to connect them to corresponding pins of J6 and J10 or the data captured will not match the HP 163X setup provided on disc. You would then need to change the HP 163X [Timing] Format Specification menu to match your hook-up.

CONNECT FRONT PANEL OUTPUTS

If you want any data or control lines connected to the front panel outputs, use the single jumper wires to connect pins of J7 to pins of J5. See figure 5-1. When using the mass-connect jumper cable the signals at J7 correspond to the mnemonics at J6.

For example: To connect TCK to front panel Output 1, connect a jumper between J7 pod 1 pin 0 (top right) and J5 pin 1.

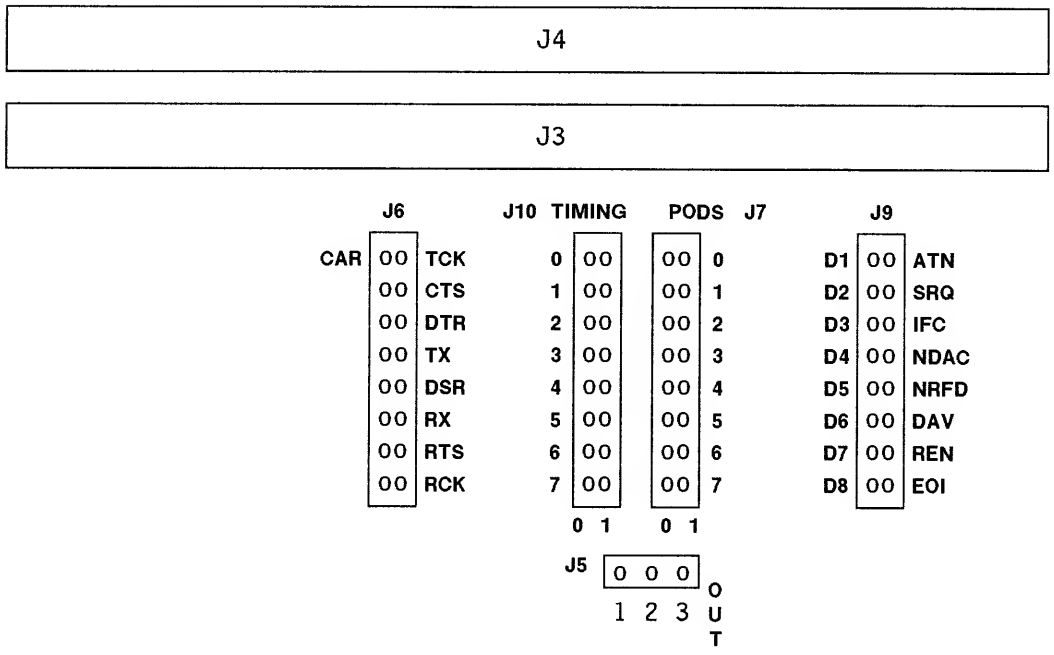


Figure 5-1. RS-232-C Timing Connector Locations.

SET DTE/DCE SWITCH Set the DTE/DCE switch (left side of PC board) to the position corresponding to the desired sync transmit clock. If the transmit clock from the terminal (computer) is desired use DTE and if the transmit clock from the modem is desired use DCE.

INSTALL PREPROCESSOR Once all the connections are made, place the HP 10342B at the bottom of the HP 10269B and connect the two 60-pin cables to the connectors on the HP 10342B. Fit the HP 10342B into the bottom of the HP 10269B and fasten them together with the two captive screws.

FRONT PANEL SWITCHES Set the front panel switches depending on the protocol, parity, etc. of the bus you are working with. The HP 10342B needs the proper protocol settings to disassemble the data on the bus.

BIT In BIT PROTOCOL (BOP, bit oriented synchronous protocol), the only other switch setting that must be made is 8 ASCII or 8 EBCDIC in BITS/CHAR. No other switch selections are relevant because the rest of the protocol is predefined. Clock comes from the external source, either terminal (DTE) or modem (DCE).

CHAR In CHAR PROTOCOL (BCP, byte control synchronous protocol), the PARITY and BITS/CHAR switch settings must be set so that the HP 10342B knows which characters to sync on. These sync characters are not displayed due to internal processing in the HP 10342B. Clock comes from the external source, either terminal (DTE) or modem (DCE).

ASYNC When ASYNChronous is selected, the settings of all other front panel switches are relevant. The clock source is from the internal source, ASYNC BITS/SEC.

The PARITY must be set.

The BITS/CHAR must be set.

ASYNC BITS/SEC must be set.

When transmit or receive data is present a state will be stored. Lack of data, or improper sync characters, results in a slow clock indication from the logic analyzer.

Probe Interface

Either an HP 10269B or HP 10269A can be used with the HP 10342B. The HP 10269A does not support the additional 8 timing channels of the HP 1630D. Since the HP 10342B provides nine timing channels, the CAR (Carrier Detect) line is dropped for eight-channel timing.

POD CONNECTOR OVERLAY — Lay the HP 10269B overlay over the pod connectors. If you are using an HP 10269A the overlay will be too large to fit well. The overlay shows where pods connect for various logic analyzers and bus preprocessing. It also gives other useful information.

CONNECT PODS — Connect the logic analyzer pods to the connectors on the HP 10269. If you are using an HP 10269B follow the overlay. For an HP 163XD, POD 2 connects to connector A, POD 3 to B, POD 1 to E, and POD 0 to connector I. If you are using an HP 163XA/G there is no POD 0. If you are using an HP 10269A the connections are the same except there is no POD connector I.

If you are using the HP 10342B on both RS-232-C and HP-IB, you can connect logic analyzer POD 4 to pod connector D. You can then switch to HP-IB processing by moving POD 3 to connector C and loading the HP-IB inverse assembler and configuration files.

CONNECT POWER — Connect the BNC cable supplied with the HP 10269B between the +5V input of the HP 10269B and the +5V output of the logic analyzer.

CONNECT RS-232-C CABLE — Connect the RS-232 ribbon cable between the bus to be monitored and the RS-232C/V.24 connector on the HP 10342B.

System Operation

Be sure all the addresses are set on the peripherals before you apply power, since most address switch settings are read on power-up.

APPLY POWER — Turn on power for all equipment involved. The logic analyzer comes up in the [Configuration] menu of the System Specification. Press the PREV[ ] key to get the [Storage Operations] menu.

CHECK FOR DISC — Press INSERT to check for the disc drive and display the disc file directory.

LOAD INVASM — ROLL the list up to point to the desired file to load. The inverse assembler must be loaded first, so load "IRS232C invasm" by pointing to it, selecting [Load] for an Operation, and pressing INSERT.

LOAD CONFIG — Next, load the configuration file "IRS232C config" or "IRS232G config" depending on your logic analyzer. The instrument will not load the wrong one.

RUN — Press RUN. As soon as data is available on the bus the logic analyzer will begin to accumulate data.

You may modify the logic analyzer menus to suit the measurement you need to make. Consult your logic analyzer Operating Manual for further information.

SIGNAL CONNECTIONS

The HP 10342B provides processed data and status to the logic analyzer state inputs. The timing inputs are buffered from the RS-232-C bus except for TX CLK and RX CLK which are selected in the HP 10342B.

Table 5-1. Logic Analyzer to RS-232-C Signal Connections.

	STATE[1]		
	HP 10269B[2]		HP 163X
SIGNAL	CONN	PIN	POD
Clock	A	L CLK	2
	A	0	
	A	1	
Serial	A	2	
Data	A	3	
Converted			
to	A	4	
Parallel	A	5	
	A	6	
	A	7	2
TX/RX	B	0	3
CC LSB	B	1	
CC MSB	B	2	
CTS	B	3	
DSR	B	4	
RTS	B	5	
DTR	B	6	
CD	B	7	3
TIMING			
TX CLK[3]	E	0	1
CTS[4]	E	1	
DTR[4]	E	2	
TX[4]	E	3	
DSR[4]	E	4	
RX[4]	E	5	
RTS[4]	E	6	
RX CLK[3]	E	7	1
CAR[4,5]	I	0	0

1. Processed through SIO in HP 10342B
2. Same for HP 10269A except no pod connector I (POD 0).
3. Clock selected in HP 10342B
4. Signal from buffered RS-232-C lines.
5. HP 163XD only and HP 10269B only.

Clock

One clock is supplied to the logic analyzer from the processor in the HP 10342B. This clock is provided to POD 2 and is the L Clock. The logic analyzer clocks data on the negative edge of the L Clock.

Data

The Data, at HP 10269 connector A (logic analyzer POD 2), is the parallel format of the serial data byte. It has been processed in the SIO (Serial IN/OUT Interface) and processor of the HP 10342B.

Status Byte

The Status Byte, at Connector B of the HP 10269, is provided by the processor in the HP 10342B.

Bit 0 represents whether the data is transmitted (1) or received (0) and is used by the inverse assembler.

Bits 1 and 2, CC LSB and CC MSB, represent front panel settings for BITS/CHAR and are used by the inverse assembler to interpret data.

00 = Normal Character
01 = EBCDIC Character Set
10 = 6-bit Transcode Character Set
11 = Not Used

Bits 3-7 are the handshake signals. They have been processed in the SIO in the HP 10342B and represent the status of the handshake lines for each serial data byte.

Timing Signals

For further information about the timing signals see text and partial schematics following SCHEMATICS in Chapter 2.

Most timing signals are buffered directly from the RS-232-C bus. The TXCLK and RXCLK are clocks selected in the HP 10342B by the DTE/DCE switch and front panel set-up.

The Carrier Detect (CAR) is also buffered directly from the RS-232-C bus. The CAR timing signal is not available when using a factory configured HP 10342B with the HP 163XA, HP 1630G, or the HP 10269A.

The timing signals supplied to the logic analyzer are of the opposite sense compared to the mark/space definition in the RS-232-C standard (see figure 5-2). The line receivers buffer, invert, and convert the RS-232 signals to TTL. The logic analyzer timing inputs are not designed to handle the ±25V signals specified by RS-232-C, so they are connected to the buffered signals.

Though the timing signals are of the opposite sense to that defined by the RS-232-C specification, they are of the same sense as the signals supplied to the RS-232 line drivers in the DCE. This makes it easier to compare the output (TTL) of the asynchronous receiver/transmitter in the DCE to the TTL signal applied to the SIO in the DTE.

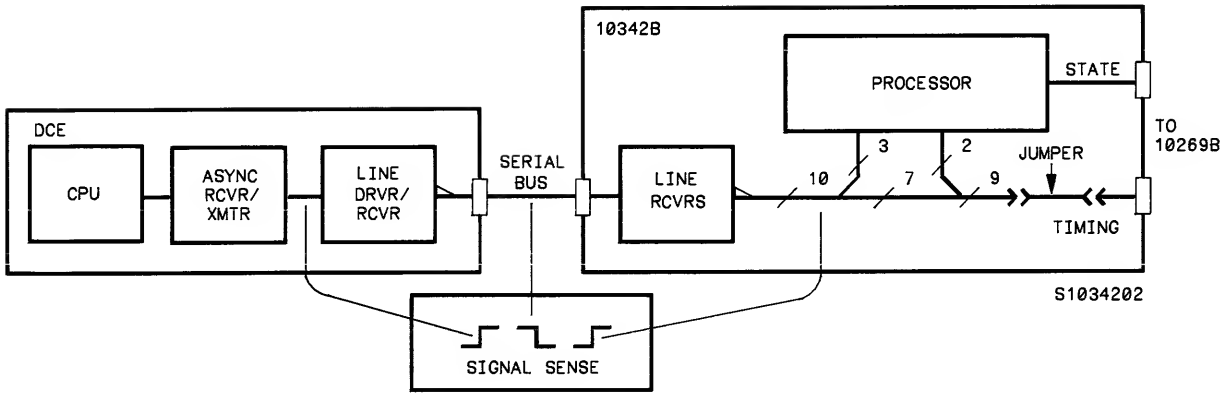


Figure 5-2. Signal Sense Diagram.

ADDRESS (ADDR)

There is an Address (ADDR) label set up in the [State] Format Specification with one bit from a pod assigned to the label . There is no RS-232-C information in this label. The label is necessary for operation of the logic analyzer but not for use with the HP 10342B. If the ADDR label appears on screen you can go to the [State] List menu and move it off the screen using the SHIFT and ROLL keys. This is done by the configuration file when the software is loaded.

MNEMONICS

The HP 10342B inverse assembler for RS-232-C uses the common mnemonics rather than the mnemonics specified in the EIA Standard. Table 5-2 provides a cross reference.

Table 5-2. RS-232-C Mnemonic Cross Reference.

PIN	MNEMONIC	
	COMMON	RS-232-C
2	TX	BA
3	RX	BB
4	RTS	CA
5	CTS	CB
6	DSR	CC
8	CD	CF
15	DCE CLK	DB
17	REC CLK	DD
20	DTR	CD
24	DTE CLK	DA

SYNC CHARACTERS

The HP 10342B must receive the proper sync characters in order to process data. The SIO is programmed to recognize the standard sync characters for the selected character code. If some other sync characters are being sent the logic analyzer will display "Slow Clock".

The only place the transmitted sync character can be seen is in the timing display. The HP 10342B does not provide the sync characters to the state display. Table 5-3 shows the expected sync characters for given character codes.

Table 5-3. Standard Sync Characters.

CHAR CODE	SYNC CHAR
6 BIT TRANS	3A3A HEX
7 BIT ASCII	1616 HEX
8 BIT ASCII	1616 HEX
8 BIT EBCDIC	3232 HEX

The SIO recognizes a 16-bit "character word". When observing the sync character data string, the relationship of this word to the idle characteristics of the data line and the parity of the transmitted data must be taken into account. This is shown further in the following two examples.

When observing bit strings on the timing channels of the logic analyzer note that data is clocked on the rising edge of TX CLK or RX CLK.

7-BIT ASCII
(no parity)

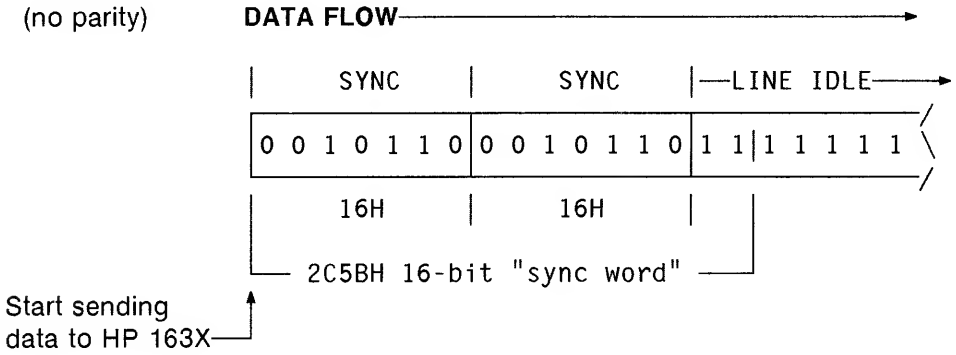


Figure 5-3. 7-Bit ASCII Sync Sequence.

As can be seen, the SIO uses two "bits" from the idle bus to fill out the two "missing" bits of the character. It then uses 2C5BH as a comparison to recognize the sync characters. If the bus does not idle high (idle high is standard) the sync characters will not be recognized.

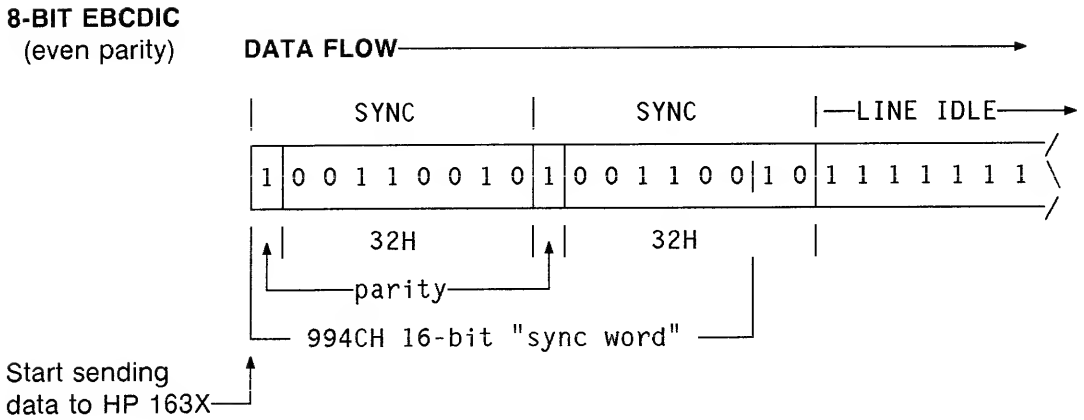


Figure 5-4. 8-Bit EBCDIC Sync Sequence.

Here the sync characters with parity have a longer bit string than the "sync word". The two least significant bits are dropped and the SIO uses 994CH as a comparison to recognize the sync characters.

BLOCK CHECK CHARACTERS

Tha last two characters of the data stream are Block Check Characters (BCC). These characters are actually CRCs and are passed on to the logic analyzer as data. However, they have been altered by the SIO and their value is no longer significant.

Chapter 6
RS-449 BUS PREPROCESSING

INTRODUCTION

The RS-449 is a serial interface with balanced data and control lines. A brief overview of RS-449 is given in Appendix D. A comparison between several of the serial interfaces is provided in Appendix B.

PREPROCESSOR FUNCTION

The RS-449 has two categories of interchange circuits, Category I and Category II. Category I circuits are the high-speed circuits and are balanced. Category II circuits are low-speed, unbalanced and used for secondary functions. The HP 10342B processes only the Category I circuits.

The primary function of the HP 10342B is to convert the serial data stream into parallel data and status. It monitors five handshake lines and stores their states for each character. Four of the handshake lines are synchronous with the serial controller and one line (carrier detect) is asynchronous but sampled each time a character is output to the logic analyzer.

All lines are buffered at the input to the HP 10342B. The buffers provide one RS-449 standard load to the bus. Signals are inverted by the buffer circuitry.

The HP 10342B provides a mass-connect feature for connecting the bus lines to timing channels, or individual connections can be made with jumper wires provided. Timing connections are made to the buffered and inverted signals.

Additionally, any buffered line can be connected to one of the three HP 10342B front panel outputs provided. These can be used for connection to an oscilloscope or one of the analog channels or trigger of an HP 1631A/D.

SYSTEM SET-UP

The minimum equipment necessary to use the HP 10342B Bus Preprocessor is as follows:

Logic Analyzer: HP 1630A/D/G* or HP 1631A/D*
* with HP 1630/31A or HP 1630G only 8 timing channels are available
Probe Interface: HP 10269A* or HP 10269B
* with the HP 10269A only 8 timing channels are available
Disc Drive: HP 9121D/S or HP 9122D/S
HP-IB cables for peripherals
HP 10342B Bus Preprocessor

Use the following step-by-step procedure to set up the system for RS-449 preprocessing.

Logic Analyzer

SET UP SYSTEM

Set up your logic analyzer system using procedures in your equipment operators manuals. Set-up will depend on the equipment and peripherals you are using.

Bus Preprocessor

The HP 10342B comes from the factory set up for processing HP-IB.

CONNECT TIMING JUMPER

On the HP 10342B, connect the ribbon jumper cable to the appropriate pins. All 16 possible timing channels are connected when the jumper cable is connected from J6 to J10. Only nine channels are used with RS-449 processing. See figure 6-1.

If you use the single jumper wires to connect the timing signals be sure to connect them to corresponding pins of J6 and J10 or the data captured will not match the HP 163X setup provided on disc. You would then need to change the HP 163X [Timing] Format Specification menu to match your hook-up.

CONNECT FRONT PANEL OUTPUTS

If you want any data or control lines connected to the front panel outputs, use the single jumper wires to connect pins of J7 to pins of J5. See figure 6-1. When using the mass-connect jumper cable the signals at J7 correspond to the mnemonics at J6.

For example: To connect TCK to front panel Output 1, connect a jumper between J7 pod 1 pin 0 (top right) and J5 pin 1.

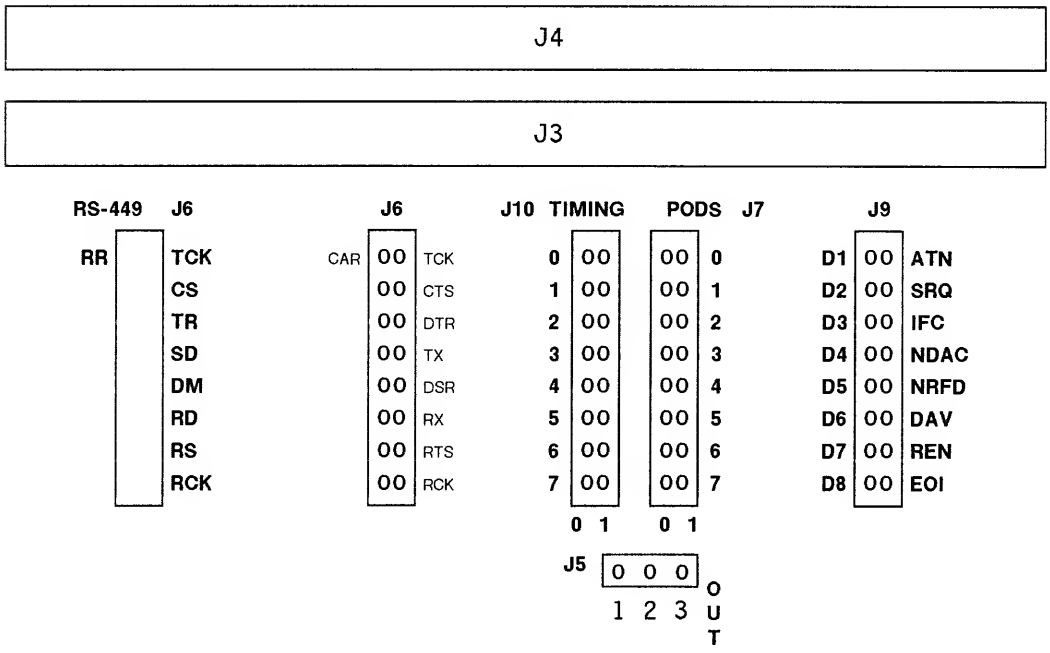


Figure 6-1. Timing Connector Locations.

SET DTE/DCE SWITCH Set the DTE/DCE switch (left side of PC board) to the position corresponding to the desired sync transmit clock. If the transmit clock from the terminal (computer) is desired use DTE and if the transmit clock from the modem is desired use DCE.

INSTALL PREPROCESSOR Once all the connections are made, place the HP 10342B at the bottom of the HP 10269B and connect the two 60-pin cables to the connectors on the HP 10342B. Fit the HP 10342B into the bottom of the HP 10269B and fasten them together with the two captive screws.

FRONT PANEL SWITCHES Set the front panel switches depending on the protocol, parity, etc. of the bus you are working with. The HP 10342B needs the proper protocol settings to disassemble the data on the bus.

BIT In BIT PROTOCOL (BOP, bit oriented synchronous protocol), the only other switch setting that must be made is 8 ASCII or 8 EBCDIC in BITS/CHAR. No other switch selections are relevant because the rest of the protocol is predefined. Clock comes from the external source, either terminal (DTE) or modem (DCE).

CHAR In CHAR PROTOCOL (BCP, byte control synchronous protocol), the PARITY and BITS/CHAR switch settings must be set so that the HP 10342B knows which characters to sync on. These characters are not displayed due to internal processing in the HP 10342B. Clock comes from the external source, either terminal (DTE) or modem (DCE). Parity must be specified as shown in the following table.

ASYNC When ASYNChronous is selected, the settings of all other front panel switches are relevant. The clock source is from the internal source, ASYNC BITS/SEC.

The PARITY must be set.

The BITS/CHAR must be set.

ASYNC BITS/SEC must be set.

When transmit or receive data is present a state will be stored. Lack of data results in a slow clock indication from the logic analyzer.

Probe Interface

Either an HP 10269B or HP 10269A can be used with the HP 10342B. The HP 10269A does not support the additional 8 timing channels of the HP 1630D. Since the RS-449 only uses nine timing channels, the RR (Receiver Ready) line is dropped for eight-channel timing.

POD CONNECTOR OVERLAY — Lay the HP 10269B overlay over the pod connectors. If you are using an HP 10269A the overlay will be too large to fit well. The overlay shows where pods connect for various logic analyzers and bus preprocessing. It also gives other useful information.

CONNECT PODS — Connect the logic analyzer pods to the connectors on the HP 10269. If you are using an HP 10269B follow the overlay. For an HP 163XD, POD 2 connects to connector A, POD 3 to B, POD 1 to E, and POD 0 to connector I. If you are using an HP 1630A/G or HP 1631A there is no POD 0. I you are using an HP 10269A the connections are the same except there is no POD connector I.

If you are going to be using the HP 10342B on both RS-449 and HP-IB, you can connect logic analyzer POD 4 to pod connector D. This will allow you to switch to HP-IB processing by moving POD 3 to connector C and loading the HP-IB inverse assembler and configuration file.

CONNECT POWER — Connect the BNC to BNC cable supplied with the HP 10269B between the +5V input of the HP 10269 and the +5V output of the logic analyzer.

CONNECT RS-449 CABLE — Connect the RS-449 ribbon cable between the bus to be monitored and the RS-449 connector on the HP 10342B.

System Operation

Be sure all the addresses are set on the peripherals before you apply power, since most address switch settings are read on power-up.

APPLY POWER — Turn on power for all equipment involved. The logic analyzer comes up in the [Configuration] menu of the System Specification. Press the PREV[ ] key to get the [Storage Operations] menu.

CHECK FOR DISC — Press INSERT to check for the disc drive and display the disc file directory.

LOAD INVASM — ROLL the list up to point to the desired file to load. The inverse assembler must be loaded first, so load "IRS449 invasm" by pointing to it, selecting [Load] for an Operation, and pressing INSERT.

LOAD CONFIG — Next, load the configuration file "IRS449 config" or "IRS449G config" depending on your logic analyzer. The instrument will not load the wrong one.

RUN — Press RUN. As soon as data is available on the bus the logic analyzer will begin to accumulate data.

You may modify the logic analyzer menus to suit the measurement you need to make. Consult your logic analyzer Operating Manual for further information.

SIGNAL CONNECTIONS

The HP 10342B provides processed data and status to the logic analyzer state inputs.

Table 6-1. Logic Analyzer to RS-449 Signal Connections.

	STATE[1]		
	HP 10269B[2]		HP 163X
SIGNAL	CONN	PIN	POD
Clock	A	L CLK	2
	A	0	
	A	1	
Serial	A	2	
Data	A	3	
Converted			
to	A	4	
Parallel	A	5	
	A	6	
	A	7	2
TX/RX	B	0	3
CC LSB	B	1	
CC MSB	B	2	
CS	B	3	
DM	B	4	
RS	B	5	
TR	B	6	
RR	B	7	3
	TIMING		
TX CLK[3]	E	0	1
CS[4]	E	1	
TR[4]	E	2	
SD[4]	E	3	
DM[4]	E	4	
RD[4]	E	5	
RS[4]	E	6	
RX CLK[3]	E	7	1
RR[4,5]	I	0	0

1. Processed through SIO in HP 10342B
2. Same for HP 10269A except no pod connector I (POD 0).
3. Clock selected in HP 10342B
4. Signal from buffered RS-449 lines.
5. HP 1630D only.

Clock

One clock is supplied to the logic analyzer from the processor in the HP 10342B. This clock is provided to POD 2 and is the L Clock. The logic analyzer clocks data on the negative edge of the L Clock.

Data

The Data, at HP 10269 connector A (logic analyzer POD 2), is the parallel format of the serial data byte. It has been processed in the SIO (Serial IN/OUT interface) and processor of the HP 10342B.

Status Byte

The Status Byte, at connector B of the HP 10269, is provided by the processor in the HP 10342B.

Bit 0 represents whether the data is transmitted (1) or received (0) and is used by the inverse assembler.

Bits 1 and 2, CC LSB and CC MSB, represent front panel settings for BITS/CHAR and are used by the inverse assembler to interpret data.

00 = Normal Character
01 = EBCDIC Character Set
10 = 6-bit Transcode Character Set
11 = Not Used

Bits 3-7 are the handshake signals. They have been processed in the SIO in the HP 10342B and represent the status of the handshake lines for each serial data byte.

Timing Signals

For further information about the timing signals see text and partial schematics following SCHEMATICS in Chapter 2.

Most timing signals are buffered directly from the RS-449 bus. The TXCLK and RXCLK are clocks selected in the HP 10342B by the DTE/DCE switch and front panel set-up.

The Receiver Ready (RR) is also buffered directly from the RS-449 bus. The RR timing signal is not available when using a factory configured HP 10342B with the HP 163XA, HP 1630G, or the HP 10269A.

The timing signals supplied to the logic analyzer are of the opposite sense compared to the mark/space definition in the RS-449 standard (see figure 6-2). The line receivers buffer, invert, and convert the RS-449 signals to TTL.

Though the timing signals are of the opposite sense to that defined by the RS-449 specification, they are of the same sense as the signals supplied to the RS-449 line drivers in the DCE. This makes it easier to compare the output (TTL) of the asynchronous receiver/transmitter in the DCE to the TTL signal applied to the SIO in the DTE.

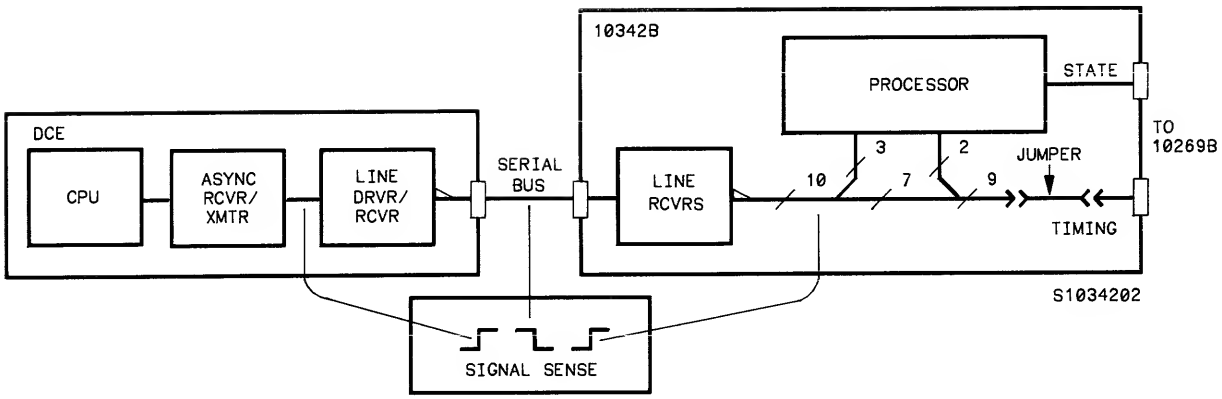


Figure 6-2. Signal Sense Diagram.

ADDRESS (ADDR)

There is an Address (ADDR) label set up in the [State] Format Specification with one bit from a pod assigned to the label . There is no RS-449 information in this label. The label is necessary for operation of the logic analyzer but not for use with the HP 10342B. If the ADDR label appears on screen you can go to the [State] List menu and move it off the screen using the SHIFT and ROLL keys. This is done by the configuration file when the software is loaded.

SYNC CHARACTERS

The HP 10342B must receive the proper sync characters in order to process data. The SIO is programmed to recognize the standard sync characters for the selected character code. If some other sync characters are being sent the logic analyzer will display "Slow Clock".

The only place the transmitted sync character can be seen is in the timing display. The HP 10342B does not provide the sync characters to the state display. Table 6-2 shows the expected sync characters for given character codes.

Table 6-2. Standard Sync Characters.

CHAR CODE	SYNC CHAR
6 BIT TRANS	3A3A HEX
7 BIT ASCII	1616 HEX
8 BIT ASCII	1616 HEX
8 BIT EBCDIC	3232 HEX

The SIO recognizes a 16-bit "character word". When observing the sync character data string, the relationship of this word to the idle characteristics of the data line and the parity of the transmitted data must be taken into account. This is shown further in the following two examples.

When observing bit strings on the timing channels of the logic analyzer note that data is clocked on the rising edge of TX CLK or RX CLK.

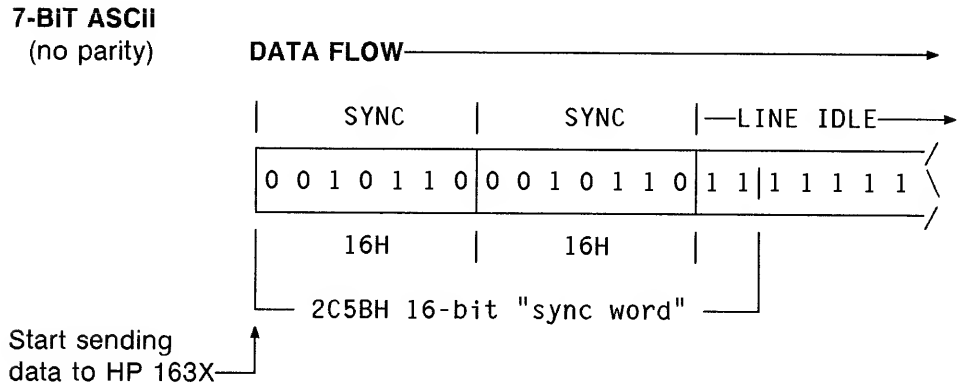


Figure 6-3. 7-Bit ASCII Sync Sequence.

As can be seen, the SIO uses two "bits" from the idle bus to fill out the two "missing" bits of the character. It then uses 2C5BH as a comparison to recognize the sync characters. If the bus does not idle high (idle high is standard) the sync characters will not be recognized.

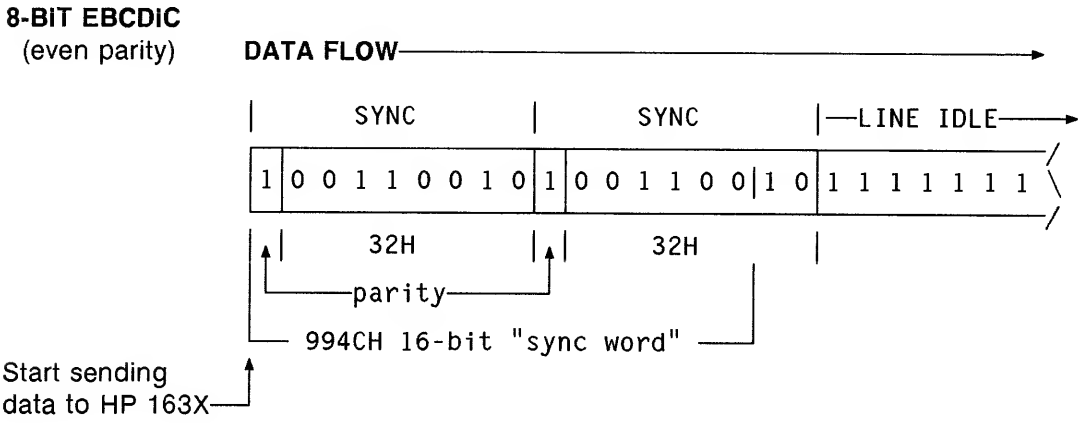


Figure 6-4. 8-Bit EBCDIC Sync Sequence.

Here the sync characters with parity have a longer bit string than the "sync word". The two least significant bits are dropped and the SIO uses 994CH as a comparison to recognize the sync characters.

BLOCK CHECK CHARACTERS

Tha last two characters of the data stream are Block Check Characters (BBC). These characters are actually CRCs and are passed on to the logic analyzer as data. However, they have been altered by the SIO and their value is no longer significant.

Appendix A
HP-IB OVERVIEW

INTRODUCTION

HP-IB is the Hewlett-Packard implementation of IEEE Standard 488-1978. The following is a brief overview of HP-IB. If additional information is needed obtain the standard from the appropriate source.

THE HP-IB

The HP-IB employs a 16-line bus to interconnect up to 15 instruments. Each instrument on the bus is connected in parallel to the 16 lines of the bus. Eight of the lines are used to transmit data and the remaining eight are used for data transfer control (handshake) and bus management. Data is transferred by means of an interlocked "handshake", permitting asynchronous communication over a wide range of data rates.

The HP-IB structure is diagrammed in figure A-1. Four types of devices may be used on the bus based on their functions: (1) devices only able to talk, (2) devices only able to listen, (3) devices able to talk and listen, and (4) devices able to talk, listen, and control.

The simplest instrument is one that only talks. When signaled this device enters its output on the data bus lines in a fixed configuration. The configuration may be altered only by front panel control.

Devices that only listen respond to data from the HP-IB data lines. In the case of a signal generator, this data could cause the instrument to output signals of different amplitude and frequency, external to the bus. Printers are frequently listen only instruments.

A digital multimeter is a device that listens and talks. The multimeter is configured by signals from the controller, takes the requested reading, and returns the results on the bus.

The controller, along with talk and listen capabilities, controls all operations on the interface bus.

As shown in figure A-1, the 16 lines of the HP-IB form three functional groups: five lines for interface management, three lines for handshake (data byte transfer) control, and eight bidirectional lines for carrying data.

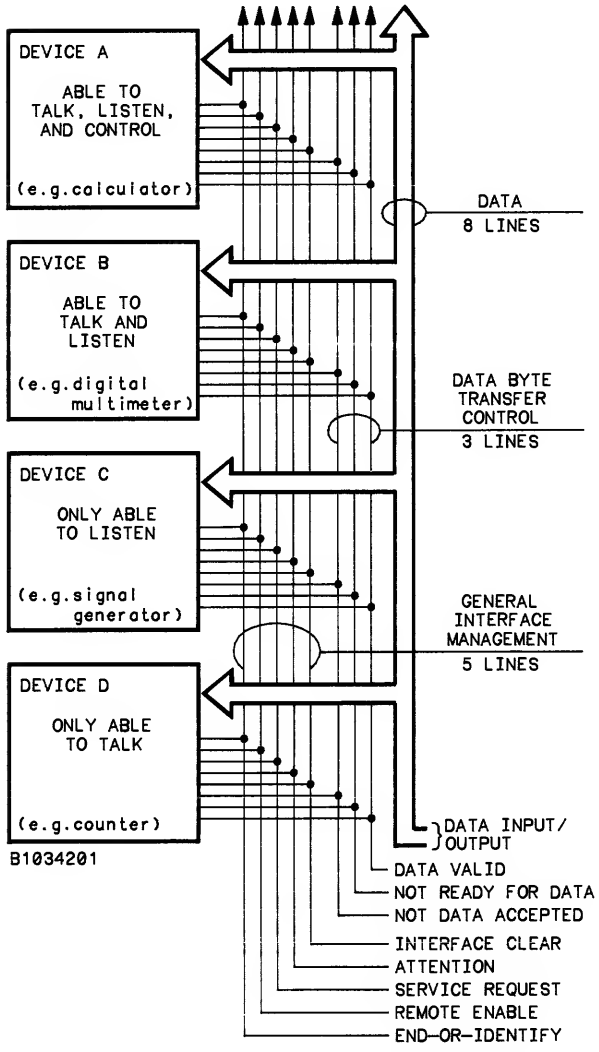


Figure A-1. HP-IB Interface Capabilities and Bus Structure.

INTERFACE MANAGEMENT LINES

1. Attention (ATN) specifies how data on the data input/output (DIO) lines are to be interpreted, and by which devices. ATN is pulled low for commands (Command Mode) and released for data by the controller.

   In command mode the controller is active and all other devices are waiting for instructions. Command Mode instructions which can be issued by the controller fall into five groups:

   a. Talker Address Group (TAG) commands enable a specific device to talk. Only one device at a time may act as the talker. When the controller addresses one device to talk, the previous talker is automatically unaddressed and ceases to be a talker.

   b. Listener Address Group (LAG) commands enable a specific device to listen. Up to 14 devices at a time may be listeners.

   c. Universal Command Group (UCG) commands cause all bus devices capable of responding to these commands from the controller to do so at any time regardless of whether they are addressed.

   d. Addressed Command Group (ACG) commands are similar to universal commands except that they are recognized only by devices that are addressed only as listeners.

   e. Secondary Command Group (SCG) commands are used when addressing extended listeners and talkers, or enabling the parallel poll.

2. Interface Clear (IFC) puts the entire system into a predefined quiescent state.

3. Service Request (SRQ) is used by a device to indicate the need for attention and to request an interruption of the current sequence of events.

4. Remote Enable (REN) in conjunction with other messages selects between alternate sources of device programming data (typically HP-IB vs front panel).

5. End or Identify (EOI) indicates the end of a multiple byte transfer sequence, or, with ATN executes a polling sequence.

The Unlisten Address Command (UNL) unaddresses all listeners that have been previously addressed to listen. The Untalk Address Command (UNT) unaddresses any talker that had been previously addressed to talk.

HANDSHAKE LINES

1. Data Valid (DAV) indicates the availability and validity of information on the data lines.

2. Not Ready For Data (NRFD) indicates the state of readiness of devices to accept data.

3. Not Data Accepted (NDAC) indicates the condition of acceptance of data by device(s).

The DAV, NRFD, and NDAC lines operate in a three-wire interlocked handshake process to transfer each data byte across an interface (figure A-2).

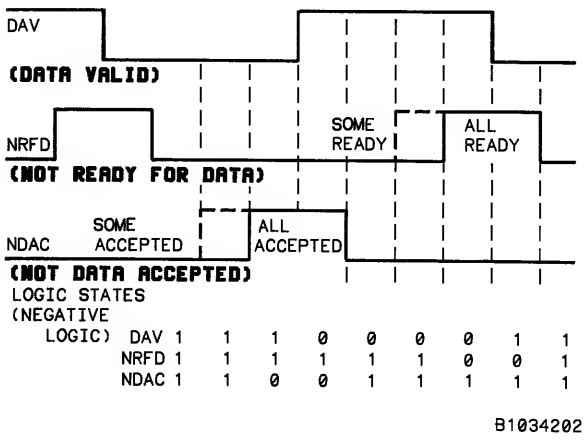


Figure A-2. HP-IB Handshake Sequence.

A handshake sequence is entered with the listener-controlled NRFD and NDAC both low. Line DAV is high. As each listener is ready to accept data, it releases its Not Ready For Data (NRFD) line. When all listeners have released the NRFD line, pull-up resistors on the line pull NRFD high. The talker signals new Data Valid by pulling the DAV line low. Listeners respond by pulling their NRFD outputs low. During the period that listeners accept data, they release the Not Data Accepted (NDAC) line. When data has been accepted by all the listeners, the NDAC line goes high. Acknowledgment by the talker releases the DAV line, and the handshake is completed by the listeners by pulling the NDAC low. A legal handshake must proceed in the manner shown in figure A-2. Note that the NRFD and NDAC lines may never go high (logic 0) together.

Appendix B
SERIAL INTERFACE COMPARISONS

INTRODUCTION

Following are several tables that show comparisons between serial interfaces covered in this document as well as interfaces not directly covered. Those not directly covered in this document are shown here for reference purposes.

Table B-1. Serial Interface Standards Comparison.

INTERFACE NAME	MECHANICAL STANDARD	ELECTRICAL STANDARD	FUNCTIONAL STANDARD
RS-232-C CCITT V.24 MIL-188C	RS-232-C ISO-2110 RS-232-C	RS-232-C CCITT V.28 MIL-188C	RS-232-C CCITT V.24 RS-232-C
RS-449 (balanced) RS-449 (unbalanced) CCITT V.35 (balanced) CCITT V.35 (unbalanced) MIL-188-114 (balanced)	RS-449 RS-449 ISO-2593 IS0-2593 MIL-188-114	RS-422 RS-423 CCITT V.11 (X.27) CCITT V.10 (X.26) MIL-188-114	RS-449 RS-449 CCITT V.24 CCITT V.24 MIL-188-114
CCITT X.20 (no clocks) CCITT X.21 (clocks) CCITT X.21-bis	ISO-4903 RS-232-C	CCITT V.11 CCITT V.10	CCITT X.27 CCITT X.26

Table B-2. Serial Interface Characteristics Comparison.

INTERFACE TYPE	INTERFACE CONNECTOR	SPEED	ELECTRICAL MAXIMUM	ELECTRICAL THRESHOLD
RS-232-C	25 pin	<20Kbps	±25V	±3V
RS-449 RS-422 (balanced) RS-423 (unbalanced)	37 pin	<10Mbps <100Kbps	±6V	±0.2V
CCITT V.35	34 pin	56Kbps	(bipolar current)	
CCITT X.20/X.21	15 pin		±10V	±0.3V
CCITT V.10 (unbalanced) CCITT V.11 (balanced)		<100Kbps <10Mbps		

Table B-3. Serial Interface Interchange Circuit Comparison.

DTE/DCE	EIA RS-232-C	CCITT V.24	EIA RS-449
	AB Signal Ground	102 Signal Ground	SG Signal Ground
→		102a DTE Common	SC Send Common
←		102b DCE Common	RC Receive Common
→			IS Terminal in Service
←	CE Ring Indicator	125 Calling Indicator	IC Incoming Call
→	CD Data Terminal Ready	108.2 Data Terminal Ready	TR Terminal Ready
←	CC Data Set Ready	107 Data Set Ready	DM Data Mode
→	BA Transmitted Data	103 Transmitted Data	SD Send Data
←	BB Received Data	104 Received Data	RD Receive Data
→	DA Transmitter Signal Element Timing (DTE Source)	113 Transmitter Signal Element Timing (DTE Source)	TT Terminal Timing
←	DB Transmitter Signal Element Timing (DCE Source)	114 Transmitter Signal Element Timing (DCE Source)	ST Send Timing
←	DD Receiver Signal Element Timing	115 Receiver Signal Element Timing (DCE Source)	RT Receive Timing
→	CA Request to Send	105 Request to Send	RS Request to Send
←	CB Clear to Send	106 Ready for Sending	CS Clear to Send
←	CF Received Line Signal Detector	109 Data Channel Received Line Signal Detector	RR Receiver Ready
←	CG Signal Quality Detector	110 Data Signal Quality Detector	SQ Signal Quality
→			NS New Signal
→		126 Select Transmit Frequency	SF Select Frequency
→	CH Data Signal Rate Selector (DTE Source)	111 Data Signaling Rate Selector (DTE Source)	SR Signaling Rate Selector
←	CI Data Signal Rate Selector (DCE Source)	112 Data Signaling Rate Selector (DCE Source)	SI Signaling Rate Indicator
→	SBA Secondary Transmitted Data	118 Transmitted Backward Channel Data	SSD Secondary Send Data
←	SBB Secondary Received Data	119 Received Backward Channel Data	SRD Secondary Receive Data
→	SCA Secondary Request to Send	120 Transmit Backward Channel Line Signal	SRS Secondary Request to Send
←	SCB Secondary Clear to Send	121 Backward Channel Ready	SCS Secondary Clear to Send
←	SCF Secondary Received Line Signal Detector	122 Backward Channel Received Line Signal Detector	SRR Secondary Receiver Ready
→		141 Local Loopback	LL Local Loopback
→		140 Remote Loopback	RL Remote Loopback
←		142 Test Indicator	TM Test Mode
→		116 Select Standby	SS Select Standby
←		117 Standby Indicator	SB Standby Indicator

Appendix C
RS-232-C/CCITT V.24 OVERVIEW

INTRODUCTION

The RS-232-C/CCITT V.24 is a serial interface standard that has predominated for many years. It originated with the requirements for teletype interface, which accounts for the large voltage specifications in the standard. It is still being designed into new equipment though it is being replaced by the RS-449 standard, due to the much higher data speeds of RS-449. The RS-232-C is the EIA standard conforming to the international standard CCITT V.24. It expands on the international standard to include the connector type, pin assignments, and electrical standards.

The following information is intended to be a coverage of the main points of RS-232-C. A person needing comprehensive information about the standard should obtain the related documents from the EIA. Many books and other documents have been written that cover RS-232-C and its many idiosyncrasies and permutations.

THE RS-232-C/CCITT V.24

Within the context of the above paragraphs, most voltage interfaces in North America conform to EIA RS-232-C. This specifies a 25-pin connector as the standard interface in datacom networks. The connector is shown in figure C-1. The interchange circuitry with pin assignments and CCITT V.24 equivalents is shown in table C-1. In addition to the mechanical and electrical requirements, it specifies an operating range of 0 to 20K bps in bit-serial operation, synchronous and asynchronous operation.

Mechanical

The signal interface between the Data Communications Equipment (DCE), usually a modem, and the Data Terminal Equipment (DTE), the remote terminal or data processor, is located at the RS-232-C specified connector located between two equipments. The female is connected to the DCE and the male to the DTE. Short cables of less than 15 meters (50 feet) are recommended, but longer cables may be used if the load capacitance is suitable. The pin assignments shown in table C-1 must be used, and unassigned pins may carry additional circuits determined by mutual agreement between the communicating parties.

While RS-232-C designates 23 circuits, the number actually used in a given application depends on the requirements of the application. In the case of some modems only nine of the 23 are used.

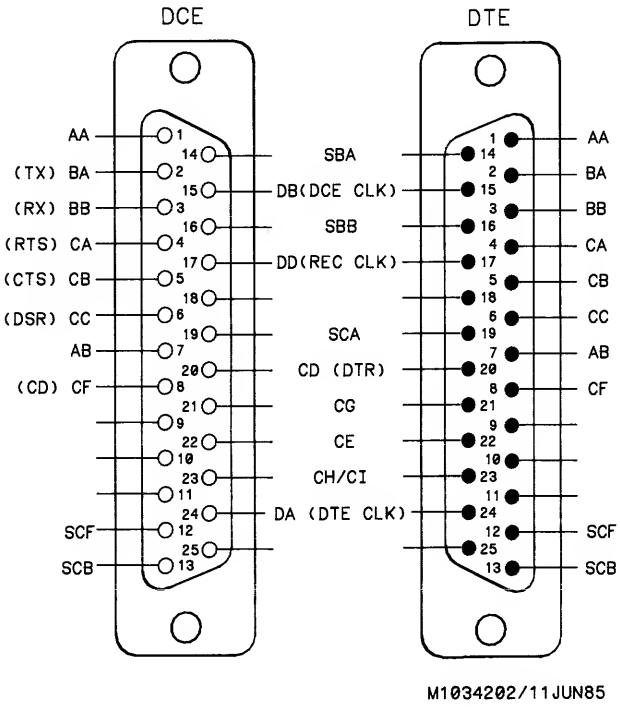


Figure C-1. RS-232-C Connector with Pin Assignments.

Electrical

Except for protective and signal grounds, all circuits carry bi-polar low-voltage signals that are suitable for electronic circuits. All voltages are measured at the connector with respect to Signal Ground (AB) and cannot exceed ±25V.

The electrical specifications are shown in table C-2.

Control circuits can be designated as fail safe. This means that when power is lost at the transmitter the receiver interprets the signal condition as off.

Table C-1. Interchange Circuits for RS-232-C and CCITT V.24 Equivalents.

PIN	DIRECTION DTE	DIRECTION DCE	RS-232-C CIRCUIT	CCITT V.24 CIRCUIT	RS-232-C DESCRIPTION
1	--		AA	101	Protective Ground
2	→		BA	103	Transmitted Data
3		←	BB	104	Received Data
4	→		CA	105	Request to Send
5		←	CB	106	Clear to Send
6		←	CC	107	Data Set Ready
7	--		AB	102	Signal Ground (Common Return)
8		←	CF	109	Received Line Signal Detector
9	--		--	--	(Reserved for Data Set Testing)
10	--		--	--	(Reserved for Data Set Testing)
11	--		--	--	Unassigned
12		←	SCF	122	Secondary Received Line Signal Detector
13		←	SCB	121	Secondary Clear to Send
14	→		SBA	118	Secondary Transmitted Data
15		←	DB	114	Transmitter Signal Element Timing (DCE Source)
16		←	SBB	119	Secondary Received Data
17		←	DD	115	Receiver Signal Element Timing (DCE Source)
18	--		--	--	Unassigned
19	→		SCA	120	Secondary Request to Send
20	→		CD	108.2	Data Terminal Ready
21		←	CG	110	Signal Quality Detector
22		←	CE	125	Ring Indicator
23	→		CH/CI	111/112	Data Signal Rate Selector (DTE/DCE Source)
24	→		DA	113	Transmitter Signal Element Timing (DTE Source)
25	--		--	--	Unassigned

Table C-2. Condensed Electrical Specifications for EIA RS-232-C.

Driver output levels with 3KΩ to 7KΩ load	$15V > V_{oh} > 5V$ $-5V > V_{ol} > -15V$
Driver output voltage with open circuit	$\|V_O\| < 25V$
Driver output impedance with power off	$R_O > 300\Omega$
Output short circuit current	$\|I_O\| < 0.5A$
Driver slew rate	$dv/dt < 30V/\mu s$
Receiver input impedance	$7K\Omega > R_{in} > 3K\Omega$
Receiver output with open circuit input	MARK
Receiver output with +3V input	SPACE
Receiver output with -3V input	MARK
+15 +5	LOGIC –0– = SPACE = CONTROL ON
+5 +3	Noise margin
+3 -3	Transition region
-3 -5	Noise margin
-5 -15	LOGIC –1– = MARK = CONTROL OFF

Appendix D
RS-449 AND RS-422 OVERVIEW

INTRODUCTION

In 1975 uniform standards were established governing the electrical parameters and interface between both high speed and low speed data communications. These standards, RS-422 and RS-423 respectively, specify those characteristics without defining the mechanical interface. RS-422 establishes characteristics of balanced voltage interface circuits while RS-423 establishes characteristics for unbalanced circuits.

The new standard for defining the mechanical and functional characteristics of the RS-422 and RS-423 standards is RS-449. This standard was released in 1977. Only the RS-422 standard will be presented further in this appendix.

THE RS-449/RS-422

The main differences between the RS-449 standard and the RS-232-C standard are the following:

1. Two connectors, a 37-pin and a 9-pin are used in place of the 25-pin connector used in RS-232-C applications. The 37-pin connector accommodates the normal interchange circuits while the 9-pin connector is used for secondary channel circuits. Both connectors are from the same family as the RS-232-C connector.

2. Depending on signaling rate, the cable distance between equipments has been extended to 60 meters (200 feet) from the RS-232-C distance of 15 meters (50 feet).

3. Ten interchange circuits not previously included in RS-232-C have been defined in RS-449.

4. The electrical characteristics (RS-422 and RS-423) in the interface have been completely re-defined. Both balanced and unbalanced type circuits may be used within one interface connection. Two categories of circuits are defined: Category I circuits, which may be balanced or unbalanced depending on data rate, and Category II circuits which are always unbalanced.

With a few additional provisions, equipment conforming to this new standard can interoperate with equipment designed to RS-232-C.

Mechanical and Functional

The basic functional characteristic of the new standard (RS-449) is operation up to a nominal limit of 2M bps in synchronous or nonsynchronous communication. The connector is shown in figure D-1 on the next page. Table D-1 shows the interchange circuits with pins, circuit names and mnemonics.

Electrical

The balanced electrical standard (RS-422) for the new interface is too involved to present here without presenting virtually the entire standard. This is because the higher data rates used with these standards requires more involved specifications. The primary points are:

1. The signal voltage levels are less than $|6V|$ open circuit and less than $|3V|$ at nominal load.

2. The receiver should require a maximum differential voltage of 200mV to assume the intended state over the common mode voltage range of -7V to +7V. The receiver should operate with a maximum differential input of 12V.

3. The nominal impedance is 100Ω and the minimum load impedance is not less than 90Ω.

4. The input impedance of the receivers should be greater than 4KΩ.

5. The short circuit current is 150mA.

6. The risetime of the data pulses is less than 0.1×(bit period) when the bit period is greater than 200ns and less than 20ns when the bit period is less than 200ns.

The unbalanced electrical standard (RS-423) is also too involved to present in this document and is only mentioned because many of the lines (Category II) are operated unbalanced at all times. The characteristics for the unbalanced signals are much the same as for the balanced signals once the lack of the differential characteristic is taken into account. Consult the EIA Standard for further information.

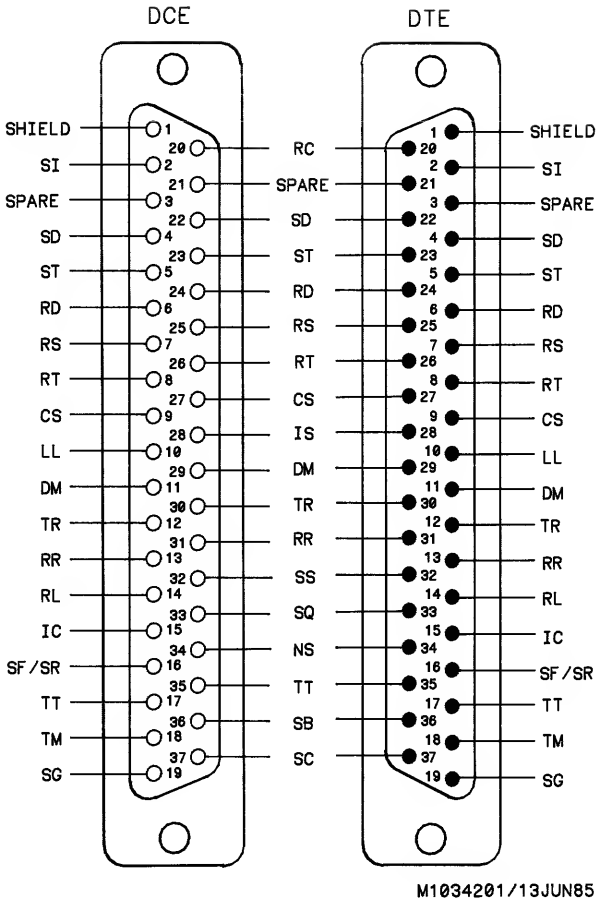


Figure D-1. RS-449 Connector with Pin Assignments.

Table D-1. Interchange Circuits for RS-449.

PINS		DIRECTION DTE DCE	CIRCUIT	CATEGORY	DESCRIPTION
1		--	SHIELD	--	--
2		←	SI	II	Signaling Rate Indicator
	20	←	RC	II	Receive Common
3		--	SPARE	--	--
	21	--	SPARE	--	--
4	22	→	SD	I	Send Data
5	23	←	ST	I	Send Timing
6	24	←	RD	I	Receive Data
7	25	→	RS	I	Request to Send
8	26	←	RT	I	Receive Timing
9	27	←	CS	I	Clear to Send
10		→	LL	II	Local Loopback
	28	→	IS	II	Terminal in Service
11	29	←	DM	I	Data Mode
12	30	→	TR	I	Terminal Ready
13	31	←	RR	I	Receiver Ready
14		→	RL	II	Remote Loopback
	32	→	SS	II	Select Standby
15		←	IC	II	Incoming Call
	33	←	SQ	II	Signal Quality
16		→	SF/SR	II	Select Frequency/ Signaling Rate Selector
	34	→	NS	II	New Signal
17	35	→	TT	I	Terminal Timing
18		←	TM	II	Test Mode
	36	←	SB	II	Standby Indicator
19		→	SG	II	Signal Ground
	37	→	SC	II	Send Common

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